Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A method including:

detecting a power management event in a system that includes a change in a system power between an external power source and a battery source~~in a system~~; and

dynamically adjusting, in response to the power management event, a voltage level and clock frequency level provided to ~~the performance states of~~ a plurality of system components including a microprocessor and system buses.

2. (Canceled) ~~The method of claim 1, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.~~

3. (Currently Amended) The method of claim 1, wherein a ~~the~~ system chipset drives the system buses.

4. (Currently Amended) The method of claim 1, ~~wherein adjusting the performance states of the system buses~~ further includes adjusting ~~the~~ a chipset buffer strength~~, the system buses supply voltages and the system buses clock frequencies~~.

5. (Currently Amended) The method of claim 1, wherein the components include ~~the~~ a memory subsystem and a ~~the~~ graphics subsystem ~~and the processor~~.

6. (Currently Amended) The method of claim 1, wherein the dynamically adjusting includes adjusting performance states ~~are adjusted~~ of the plurality of system components between a high level and a low level.

7. (Canceled) ~~The method of claim 1, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.~~

8. (Currently Amended) The method of claim 7, wherein adjusting the performance state of a ~~the~~ graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

9. (Original) The method of claim 6 ~~1~~, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state ~~(ACPI Specification C3 State)~~ upon the occurrence of the power management event to adjust the performance states of the system components.

10. (Canceled) ~~A method including:~~

~~detecting a power management event in a system ; and~~

~~automatically placing the system in a low activity state, in response to the power management event,~~

~~adjusting the performance states of a plurality of system buses, and adjusting the performance states of a plurality of system components.~~

11. (Canceled) ~~The method of claim 10, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.~~

12. (Canceled) ~~The method of claim 10, wherein the system chipset drives the system buses.~~

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13. (Canceled) ~~The method of claim 10, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.~~

14. (Canceled) ~~The method of claim 10, wherein the components include the memory subsystem, the graphics subsystem and the processor..~~

15. (Canceled) ~~The method of claim 10, wherein the performance states are adjusted between a high level and low level.~~

16. (Canceled) ~~The method of claim 10, wherein adjusting the performance state of the components includes adjusting the components supply voltages and clock frequencies.~~

17. (Canceled) ~~The methods of claim 16, wherein adjusting the performance state of the graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics~~

~~performance levels.~~

18. (Canceled) ~~The method of claim 15, wherein the low activity state is the deep sleep state (ACPI Specification C3 State).~~

19. (Currently Amended)) A system comprising:

a detector adapted to detect generation of a power management event that includes a change in a system power between an external power source and a battery source; and

a controller to automatically adjust, in response to the power management event, voltage level and clock frequency level provided to ~~the performance states of~~ a plurality of system components including a microprocessor and system buses.

20. (Canceled) ~~The system of claim 19, wherein the power of management event includes a change in the system power source from an AC outlet to a battery or vice versa.~~

21. (Currently Amended)) The system of claim 19, wherein ~~the~~ a system chipset drives the system buses.

22. (Currently Amended)) The system of claim 19, further includes adjusting a chipset buffer strength ~~wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.~~

23. (Currently Amended)) The system of claim 19, wherein the

components include ~~the processor, the~~ a memory subsystem and ~~the~~ a graphics subsystem.

24. (Currently Amended)) The system of claim 19, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level.~~wherein the performance states are adjusted between a high level and a low level~~.

25. (Canceled) ~~The system of claim 19, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.~~

26. (Currently Amended) The system of claim 2~~4~~5, wherein adjusting the performance state of ~~the~~ a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

27. (Currently Amended)) The system of claim 24~~1~~9, wherein the low activity state is the deep sleep state ~~(ACPI Specification C3 State)~~.

28. (Currently Amended) An apparatus comprising:

a detector adapted to detect generation of a power management event that includes a change in a system power between an external power source and a battery source; and

a controller to automatically adjust, in response to the power management event, voltage level and clock frequency level provided to ~~the performance states of~~ a plurality of system components including a microprocessor and system buses.

29. (Canceled) ~~The apparatus of claim 28, wherein the power of management event includes a change in the system power source from an AC outlet to a battery or vice versa.~~

30. (Currently Amended) The apparatus of claim 28, wherein ~~the~~ a system chipset drives the system buses.

31. (Currently Amended) The apparatus of claim 28, The system of claim 19, further includes adjusting a chipset buffer strength. ~~wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.~~

32. (Currently Amended) The apparatus of claim 28, wherein the components include ~~the processor, the~~ a memory subsystem and ~~the~~ a graphics subsystem.

33. (Currently Amended) The apparatus of claim 28, wherein the dynamically adjusting includes adjusting performance states of the plurality of system components between a high level and a low level. ~~wherein the performance states are adjusted between a high level and a low level.~~

34. (Canceled) ~~The apparatus of claim 28, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.~~

35. (Currently Amended) The apparatus of claim 334, wherein

adjusting the performance state of ~~the~~ a graphics subsystem includes selecting one predetermined level from two predetermined ACP Specification graphics performance levels.

36. (Currently Amended) The apparatus of claim 33 ~~28~~, wherein the low activity state is the deep sleep state. ~~(ACPI Specification C3 State).~~

37. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, the set instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event that includes a change in a system power between an external power source and a battery source~~in a system~~; and

dynamically adjusting, in response to the power management event, a voltage level and clock frequency level provided to ~~the performance states of~~ a plurality of system components including a microprocessor and system buses.

38. (Canceled) ~~The computer-readable medium of claim 37, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.~~

39. (Currently Amended) The computer-readable medium of claim 37, wherein ~~the~~ a chipset drives the system buses.

40. (Currently Amended) The computer-readable medium of claim 37, ~~wherein adjusting the performance states of the system buses~~ further includes

adjusting ~~the~~ a chipset buffer strength~~, the system buses supply voltages and the system buses clock frequencies~~.

41. (Currently Amended) The computer-readable medium of claim 37, wherein the components Currently Amended ~~the~~ a memory subsystem and a~~,~~ ~~the~~ graphics subsystem ~~and the processor~~.

42. (Currently Amended) The computer-readable medium of claim 41~~37~~, wherein the dynamically adjusting includes adjusting performance states ~~are adjusted~~ of the plurality of system components between a high level and a low level.

43. (Canceled) ~~The computer-readable medium of claim 37, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.~~

44. (Currently Amended) The computer-readable medium of claim 42~~3~~, wherein adjusting the performance state of ~~the~~ a graphics subsystem includes selecting one predetermined level from two predetermined AGP Specification graphics performance levels.

45. (Currently Amended) The computer-readable medium of claim 42~~37~~, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state ~~(ACPI Specification C3 State)~~ upon the occurrence of the power management event to adjust the performance states of the system components.